Automated IP Integration:
Gaining Cycle Time Advantage

by

Dr. Stefan Scharfenberg
Senior Staff Engineer
Motorola, SoCTD
Munich, Germany

With increasing pressure to shorten design cycle times, system integrators have realized the advantage of reusing blocks of intellectual property (IP). Today, two forces are pushing designers to optimize reuse in their designs to meet shortened cycle times. The first, miniaturization, has resulted in ever increasing chip complexity. As chip geometries have gotten smaller and smaller, designers can pack more features and IP modules into the same geography, an additional pressure on design cycle times. Ironically, this has liberated system-on-chip (SoC) designs to grow larger and larger.

The second force, consumerization, rewards first-to-market manufacturers who can optimize their design performance and feature sets and thus, capture market share. With market share, the manufacturer can realize volume production efficiencies. Thus, manufacturers continually introduce product development processes that shorten time-to-market. Consumerization has also pushed manufacturers to shorten design cycle times to as little as three to six months to offer the advanced feature sets that will retain or increase market share.

Since the rate of increasing chip complexity is outpacing design productivity, product manufacturers have recognized that rapidly integrating and reusing IP blocks are key strategies to overcome this imbalance. Reusing IP also offers system designers an avenue to overcome the apparent hurdles and expense of a rapid time-to-market design sequence.

This paper will present Motorola's IP integration flow, particularly in the context of our recently released Semiconductor Reuse Standards (SRS). The flow itself is conceptually easy to understand. See Fig. 1. However, successful reuse implementation of an IP block involves some interlocking dependencies between process steps. Effective socketization, for example, requires the IP owner's attention to the tools used to integrate the IP from a raw block through socketization, IP certification, the IP repository, and finally, integration into the final design.

[Insert Fig. 1 from white paper here.]

Reuse Standards

The SRS standards provide the playing field, the rules, and the interface methodology between stages of the IP flow. Further, these standards create the backbone for our multi-

site, multi-technology global development community. Automated tools provide the infrastructure for Socketization and Repository, while the Certification and Integration steps have partially automated tools currently available.

At the beginning of the design process, any SoC design team will map out the IP blocks to be included. These IP blocks come from either internal or external sources. Regardless of the source, each IP block in the design must be socketized. This means that it must be prepared for optimized integration in conformity with the SRS.

Socketization

SoC designs can incorporate modular IP blocks that are either fully customized (hard IP), fully synthesizable (soft IP), or a hybrid of both approaches. The IP creator's objective is to create blocks that system designers (the customers) can successfully integrate into their design. To properly integrate the IP block, the system designer will require a set of "views." Only the IP creator has sufficient knowledge of the IP to create these views, eliminate false paths during timing characterization, and determine the correctness of the results.

These views provide the designer with the appropriate information to reuse and integrate the block into the design. A capable View Generation System (VGS) will create and provide the designer these views ready for use by the integration tool. IP creators and designers have successfully used VGS to characterize a number of Motorola cores and large blocks. However, creating a package of views requires knowledge in three areas: The IP Integration System, the standard cell synthesis library, and the IP itself. The following outline summarizes the points required in each of these areas:

1. IP Integration System
    - list of tools and views
    - naming convention of views and directories
    - directory structure
    - special data formats, e.g., format of compiled and protected simulation models
    - platform dependent data
2. Standard cell synthesis library
    - list of PVT points
    - measure thresholds for delays and slopes
    - layer list for physical layout (DRC, LVS)
    - naming convention of sub circuits
3. Knowledge about the IP block
    - specifications
        - operating temperature range
        - operating voltage range
        - output loads that can be driven
        - input slopes that can be tolerated
        - clock frequency
    - clock tree recognition

- false path elimination
- verification of characterization results

Ideally, the CAD system will already be properly configured to automatically provide the required views in a plug-and-play way. The VGS system performs all of the tasks associated with the IP integration system (#1 above) and the standard cell synthesis library (#2 above). Rules to cover these two task areas are built into the system or configured using configuration files. These rules are based on our Semiconductor Reuse Standard. The tasks in the Knowledge about IP (#3 above) area are partially automated by using template forms and template configuration files.

Timing Characterization

The integration flow process that incorporates a block of reusable IP into a new design depends heavily on timing characterization. These timing views meet a variety of purposes:

- Digital timing simulation
- Synthesis of the surrounding logic
- Static timing analysis of the SoC
- Timing driven place and route

Our design flow automation process recognized that timing characterization is a natural extension of the IP creator's analysis approach. To meet these needs, we developed a timing characterization flow using Synopsys' transistor-level static timing tool, Pathmill, and gate-level timing tool, PrimeTime.

Simulation Models & Other Views

VGS also generates compiled and protected digital simulation models. Pre-compiled simulation models integrate into the target design environment more easily. Compiled simulation models can be generated from either the behavioral or gate level description and are platform and operating system dependent.

The VGS also generates many small files that are nonetheless important for seamless integration into the target SoC design environment. These views include the following: Verilog stub model, Eel (Edif external library) file, black-box ATPG model, and TLF and CLF files for place and route files. In some cases, the fully socketized IP block can bypass certification and the repository steps and be immediately integrated. The complete list of views that comprise the IP block deliverables can be found in the recent public release (December 1999) of the Semiconductor Reuse Standards.

IP Certification

Certification determines whether an IP block is reusable. It also provides metrics that indicate the quality of the block for reuse. Most of the certification is done before the IP enters the IP Repository. Additional certification may be done while the IP is in the

repository. We use the Interra product called Spyglass, which operates much like a spell checker to check the block for compliance with the Semiconductor Reuse Standards for each view. The certification team uses the VGS to test for consistency between IP views and also tests for compatibility with tools, libraries, and hardware platforms. And finally, the team also prepares a prediction of the quality and reliability of the IP block (deliverables, usage, and defect history), also called "grading."

IP Repository

The IP Repository provides an infrastructure where IP creators can offer and system designers (IP users) can acquire IP blocks for reuse. The repository system allows participants to share information in the form of Soft/Firm/Hard IP of many different types. The repository provides global access for our multi-site development community of system integrators. It allows these integrators to quickly and easily search, select, and integrate available IP blocks into their designs. The repository infrastructure consists of:

- Multiple IP vault servers that store the IP and deliverables
- A meta data relational database for easy search by a variety of user-selected parameters
- The meta database also initiates downloads from the appropriate vault server
- A web application server to query the database and generate results on a webpage

The Repository also allows IP creators to upload blocks including all deliverables into the IP vault and also upload the necessary meta data to the meta data server. The creator can use a special GUI (graphical user interface) to configure new data or edit existing meta data files.

IP Integration

We have created a common global design environment based on the capabilities of the best-in-class design and analysis tools. The design environment supports an ASIC style synthesis and integration flow. All supported tools in the design flow are encapsulated and have a graphical user interface (GUI) which simplifies usage for an inexperienced user. This environment also flexibly supports multiple technologies and synthesis libraries.

This environment supports all of our major core architectures and main IC design areas and includes a full set of user documentation and tutorials. Our mission has been to integrate inherent support for industry design and reuse standards and our internal Semiconductor Reuse Standards (SRS). SRS version (2.0) was released to the public in December of 1999 and covers 11 areas, of which the following areas have been released to the public:

- IP Block Deliverable Standards
- Documentation Standards
- HDL Coding Standards
- Peripheral Interface Standards/IP Bus Specification

Summary

IP creators and IP consumers (system integrators) now face accelerated design cycle times as short as three to six months. To accomplish this task in the face of continually smaller chip geometries requires an integration methodology. As a logical evolution from our internally developed Semiconductor Reuse Standards, we developed an IP integration flow from selection of the IP block through socketization, certification, repository, and integration. Best-in-class design and analysis tools automate many of these steps in our current design environment and further automated steps are in development. With this approach, we have developed a multi-user, multi-technology worldwide design environment equipped with GUI interfaces for ease-of-use by even novice users.

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