Design Interoperability Calls On Format Neutral Design Chain Management

by

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New internet-based Design Chain Management tools conquer the four most significant problems facing OEM electronic design teams: EDA tool interoperability, efficient use of legacy designs, low quality technical data, and irrelevant product change notices. Portable design teams typically work in the most extreme design cycle environments in the electronic design community. Design cycle pressures simply magnify the impact of these design hurdles.

The first of these hurdles, EDA tool interoperability, hasn't existed in the past because of the proprietary barriers erected and maintained by individual tool vendors. By using a "neutral" file format, these new translators convert all proprietary data into files accessible by any leading design tool. The second, efficient use of legacy design data, has remained an unrealized dream as well. Again using "neutral file formats," design teams can now realistically integrate legacy design files into current CAD-ready files. The third, low quality data, conceals high hidden costs often overlooked in the design process. These costs include data transcription errors, shifting data sources, inefficient part search and selection, and errors matching components with compatible software. The fourth, irrelevant product change notices, overwhelm design and manufacturing teams with a daily flood of emails. Design Chain Management solutions now effectively address these problems. As a result, design teams can substantially accelerate their time-to-market, reduce errors, and dramatically slash development costs.

EDA Tool Interoperability

One of the underlying industry trends that have compounded interoperability problems is outsourcing and corporate acquisitions. Today's design chain rarely resembles the monolithic, integrated design team of old. In today's high-end design flows, the portable design-chain often includes multiple outsourced participants with up to 150 tools and methodologies to reach design completion. (1)

The engineering community has pushed for tool interoperability for as long as EDA tool vendors have maintained proprietary tools. Although the EDA community is currently optimistic about industry efforts by the leading tool vendors, many prior initiatives have faltered. Curiously, tool vendor induced hurdles to interoperability chew up the budgets of design companies. A recent survey showed that design companies only spend 25% of the money budgeted for EDA on new tool purchases. EDA maintenance, training,

support, interfaces, and internal CAD development accounted for the lion's share of the budget. (2)

As these numbers suggest, portable design teams face significant EDA costs beyond tool purchases. One leading EDA vendor reported that OEM design teams spent $7 to $9 billion annually just to help EDA tools work together. The vendor further noted that for every dollar spent on tools, tool users spent an additional $3 to $5 integrating them, confirming the high costs to achieve some measure of interoperability. (3)

These burdensome indirect EDA tool costs represent not only dollar costs, but design cycle penalties as well. A leading electronics industry player reported that every week saved during the design cycle increases the revenue opportunity by an average of $50 million. (See Fig. 1) It's clear that the entire electronics industry recognizes tool interoperability as a crucial design cycle issue, but it's particularly magnified for OEMs managing often far-flung portable design-chains.

The Legacy Reuse & Data Error Problems

The electronics industry faces a continually widening gap as chip performance has outpaced the productivity advances of increasingly complex EDA tools. One widely publicized strategy for accelerating time-to-market is design reuse. Eventually, open standards groups may arrive at either design standards and/or electronic design data formatting standards that will fully and universally support design reuse. These movements still have to overcome the proprietary interests of EDA tool vendors who have derailed multiple prior initiatives.

However, these initiatives provide no current help for portable design teams seeking to implement reuse with their existing legacy designs. Designing with reuse in mind requires more initial design effort than simply executing a single project design. The payoff, although well documented by many reuse experts, can be elusive when working under critical time-to-market deadlines. Part of the problem is that legacy designs may not be in compatible EDA tool formats, symbols may have changed, and/or components may now be configured differently. Additionally, the current design team may be working with tools that are now incompatible with the formats of the original design. This suggests that at least part of the legacy design reuse problem is a subset of the overall EDA tool interoperability hurdle.

Likewise, design teams face an extensive and often hidden set of data error problems. For example, EDA tools today are so complex that design teams typically employ one tool interface programmer or system administrator for every five engineers. As a result, actual design accounts for less than half the time of the design cycle. Most of the "non-design" time is spent moving data from one tool to another. (4)

The designer may not be spending much time actually designing. Support tasks such as entering and verifying symbol data still tie up far too much of a designer's time. Component vendors have used the Internet to distribute component data sheets

electronically, reducing or eliminating the delays between updates. The advance of the Internet however, failed to ease the designer's job of actually incorporating a component into a design.

Designers still manually enter logic-symbol information into their CAD packages and proof it for errors. A project designer must repeat these steps for every component in the design. Advancing geometries and chip performance have resulted in more complex components and smaller component footprints, suggesting that this error-prone drudgery is only going to worsen. Typographical errors entered at this stage of the design can produce "board spins" or other costly late-stage corrective actions that slow a product's time-to-market.

The Flood of Product Change Notices

OEMs often outsource production to one or more contract manufacturers. Because of the large number of components on multiple projects, a typical design-engineering manager at a contract manufacturer will be bombarded with up to 400 Product Change Notices (PCNs) daily. The barrage of information is not project specific but rather component vendor specific. Large component vendors with hundreds of product families and tens of thousands of part numbers publish a regular flood of product change notices.

Most of the changes aren't relevant to current manufacturing projects. Typical handling of product change notices is to ignore them until a product fails in test. Despite the costs associated with a relevant product change notice, many manufacturing operations find it more efficient to catch assembled board failures during test and then backtrack. The costs of solving a parts change problem include: rush inspections of in-process inventory, rework of assembled parts, additional purchasing time to find enough obsolete parts to retrofit existing assemblies, associated component engineering time, and disruption of design and/or manufacturing flows.

Typically, the design engineer spends a day figuring out the problem and fixes it accordingly. This turns out to be more cost-effective than maintaining a sufficiently large staff to sort through and identify relevant PCNs. For most operations, this practice is not particularly elegant, but is currently the most efficient, despite related costs.

XML Based-Infrastructure Solution

Imagine a portable design team with an advanced tool set from leading EDA vendor "C". In their design chain, they have in-house designers, a specialized outside design team for the analog portion of the design, outsourced simulation and verification houses, a board manufacturer, and a contract manufacturing assembly house.

Much to the delight of their tool vendor, the design team decides that they want all formats and all work done in their design chain on vendor "C's" tools. This fairy tale now unfortunately confronts reality, which is that the outsourced vendors have many customers working with many different tools. In short, the design team bumps into

severe obstacles implementing their policy. And even if they should miraculously implement a design chain that only included tools from vendor "C", they would still have to maintain version control. So this unlikely scenario is likely to fall flat on its face.

And even if all participants use the same vendor "C", the design team still faces the daunting and error-plagued task of entering all of the component data. For instance, it may take a designer two to three weeks to enter the specifications and data for a 400-pin processor. Fortunately, new data mining solutions pull technical data out of .PDF files in format "neutral" XML.

Extensible Markup Language (XML) provides a workable infrastructure solution. The infrastructure employs a network of secure servers located at component vendors and their key customers. New data mining software captures and translates component data and symbols from .PDF files and saves them as XML. Since it's format "neutral" and operates from a standard web browser, XML files can then be readily converted into a CAD-ready form.

This elegant solution has been propelled by the electronics industry standards organization RosettaNet (www.RosettaNet.org) working in conjunction with the Silicon Industry Initiative (Si2). RosettaNet selected XML as the format "neutral" means for component vendors and OEMs to share information. RosettaNet recently validated the first of many planned technical component data exchange standards, PIP2A9. Called Partner Interface Processes ™ (PIPs™), PIP2A9 provides a detailed standard titled, "Query Product Technical Information." All participating infrastructure providers successfully demonstrated elements of the PIP2A9 standard, though one successfully validated all parts of the PIP.

Using this data acquisition infrastructure, a portable design team has nearly instantaneous access to complete component data with no delays. ChipData, a design-chain management solution provider, implements the PIP2A9 standard with additional software features. For instance, once a design team member selects a particular component using a standard desktop browser, the designer simply makes a few clicks to save the logic symbol. This schematic-capture process can then be used to readily import the CAD-ready data into popular EDA toolsets. This approach provides a dramatic improvement in both the speed and accuracy of the schematic-capture process.

These same tools can translate files from most popular toolsets into XML and store them in the design chain management system. All relevant participants in the portable design-chain can then access these neutral format symbols via standard browser. When one of the design chain participants uses toolsets from a different vendor, they can select the appropriate supported tool format and the system will convert and download the symbol. Using the same process, design teams can translate legacy files into XML files, which can then be readily converted into the toolsets used by various design-chain participants.

Reducing the PCN Flood to a Trickle

During both the development and eventual manufacturing process, the design, registered on a secure server monitors the voluminous flood of product change notices. The process automatically matches the symbols and data for PCNs with each design project on the server. Only when the server identifies a PCN relevant to a particular project are the design and production participants notified.

Conclusion

Component vendors and leading electronic OEMs are already implementing these new design-chain solutions. Some of the better-known vendor participants include ST Microelectronics, Texas Instruments, Xilinx, Intel, and many more. Many leading OEMs including IBM and Lucent are strongly recommending or requiring that component vendors provide data in this methodology. Portable design teams often experience more intensified time-to-market pressures than their non-portable design counterparts. "Format neutral" design-chain management solutions offer portable design teams a pathway to close the design gap, reduce error-prone data entry, and accelerate time-to-market.

References:

1. Tets Maniwa, "Can we talk?" EEdesign, May 29, 2000.
2. ibid.
3. Karen Bartleson, "Courage to Change the Standard," Integrated System Design, www.isdmag.com/editorial/2000/viewpoint0006.html.
4. Tets Maniwa, ibid.

[Caption for Fig. 1:]

Fig. 1: Current web-based component data searches produce results that must be re-keyed. Increasing the availability of CAD-ready data file reduces support costs and accelerates time-to-market. For example, each week earlier that a new processor component launches, a major semiconductor manufacturer realizes $50 Million in extra profit opportunity.