Clean Data with a Wide Open Eye

The world's fastest logic series, the ECLinPS-Plus™ Logic Series from ON Semiconductor, also delivers telecommunications and networking designers a wide open eye pattern. In part, the wide open eye results from the family's low jitter, for instance, running at 2 GHz, jitter is less than 1 ps rms. This extraordinarily low jitter means that even running at incredibly high speeds, ECLinPS-Plus devices deliver wide open eye patterns. The result, manufacturers and designers who take advantage of ECLinPS-Plus wide open eye know the device will deliver clean data at the end of the line.

With maximum flip-flop toggle frequencies of over 3 GHz and both propagation delays and rise and fall times as low as 100 ps, the new devices earn their title as the world's fastest. With this performance, telecommunications and networking equipment designers can utilize the new logic ICs for optimal performance as signal drivers over distance, maintain outstanding signal integrity, and if necessary, synchronize multiple data streams.

"Is it possible to deliver wider eyes and higher frequencies?" asks John Veto, Product Engineering Program Manager for Advanced ECL Products, ON Semiconductor. "Absolutely. We like to think that one of the meanings of the 'Plus' in ECLinPS-Plus is that equipment designers get higher frequencies with wider eyes. The edge in and of itself represents a transmission line propagation frequency. Preserving edges minimizes jitter. A system designer using the ECLinPS-Plus series receives its contribution as the fastest logic edge. The challenge: Preserve this edge advantage in the rest of the system."

The ECLinPS-Plus family includes nearly 80 devices, of which 23 are currently available and over 50 are scheduled to be released over the next year. Some of the new devices are direct pin-replacement upgrades to the existing ECLinPS-Lite logic family. In designing the drop-in upgrades, the company's project engineers were able to increase the speed and improve the timing performance without increasing the power. Thanks to tighter internal timing specifications, the new devices deliver advanced performance for systems that require signal integrity, high-speed clock distribution, and data-synchronization.

The Wide Open Eye

"The further the 'eye' on the oscilloscope is open, the better," says Paul Shockman, Senior Applications Engineer at ON Semiconductor. "When the 'eye' is wide open, we clearly see the rising and falling edges along with the sustained high and the sustained low. If the highs are high enough, the lows low enough, the in-between empty enough, and the edges sharp enough, the 'eye' will be wide open."

With very low jitter, fast edges, and a wide open "eye", customers have taken note. At Lucent CNS Group (Converged Network Solutions), lead design engineer Adrianus Djohan works with a team building the finest fault tolerant platform in the world. "The redundancy factor that we build into the platform means that we have two motherboards

operating synchronously. We require a hierarchical clock architecture centralized from the source on the clock card. All the outputs to loads and destinations has to be very balanced. We can't use signal dividers so we start with low frequency and multipy up in whole integers. We use a lot of buffering because most of the system is differential output."

"To operate our challenging clock architecture," Djohan continued, "we need excellent synchronicity, small skew, and low jitter. We rely on the new ECLinPS-Plus series to deliver the performance we need – especially since we guarantee our customers 99.999% availability."

Jitter & Propagation

"Propagation delays of ECLinPS Plus devices are tightly controlled," says Pete Weaver, Logic Portfolio Engineer at On Semiconductor. "The devices exhibit very fast propagation delays with minimal pin-to-pin and device-to-device skews. As system speeds of new products in the market continue to rise, these devices provide the best means of distributing multiple clocks accurately." The very first ECL devices exhibited gate delays of 1100 ps. The earlier generation ECLinPS-Lite series reduced gate delays to 350 ps. The new ECLinPS-Plus series cuts gate delays one-third to 250 ps.

And the new devices deliver outstanding jitter performance. Weaver notes that, "Jitter is the variation in propagation delays from the input to output of a device. The low jitter capability of the ECLinPS-Plus series provides the unequalled signal stability and transmission reliability crucial for high-frequency test systems."

"We recently conducted jitter evaluations on the EP16 flagship device, notes Shockman. "First, we measured the jitter without the EP16 in the circuit. Then we measured the jitter with the EP16 in the circuit. The jitter is so low that it's hard to measure. That's the good news for data systems and networks because they're searching for the world's lowest jitter contribution while still delivering as high a frequency as possible. Since unmeasurable jitter is the theoretical ideal, it appears that we're pushing this ideal."

Driving a Signal

A signal has three basic components, a rise and fall rate, amplitude, and the drive behind it. The edge of the signal, as it moves down a line, tends to degrade. "The challenge," says Paul Shockman, Senior Applications Engineer at On Semiconductor, "is to keep a sharp edge. ECLinPS-Plus has some of the fastest edges in the world. One fast edge after another results in high speed transmission. Edges determine high speed transmission, while clock rates are actually a consequence of the edge rate."

As an example, the new series MC10EP16 Differential Receiver delivers typical rise and fall times of 100 ps (min) to 200 ps (max) at 85 degrees C. When operating at 200 ps rise and fall time, the device operates at a frequency of 2.7GHz. At 100ps, the device hits 3.4 GHz.

As the operating frequencies have increased from one generation of ECL family to the next, the specified amplitude has remained constant and become an industry standard at 800 mV. The MC10EP16 boasts an 800 mV peak to peak amplitude at 1.25 Gbps Ethernet frequencies. Furthermore, it delivers a viable output swing at up to 3.5 GHz with a minimum input sensitivity of 150 mV.

The distance a device can drive a signal down a line depends in part on the quality of the medium, whether it be cable or circuit board. A simple rule applies: Better cables cut line loss. For long-distance driving over coaxial cable, the ECLinPS-Plus series features a special Coaxial Cable Driver, the MC10EP89. With maximum transmission amplitude of 1400 mV, it still responds to 150 mV signals and can drive a signal thousands of feet, even miles depending on cable quality. This device features preliminary edge rates of 230 ps rise and 210 ps fall @ 85° C with a 1.4V swing in amplitude, measured at maximum clock rate.

Power Dissipation (P_D)

By its very design, Bi-Polar ECL technology exhibits higher power. As the frequency changes in the ECL power dissipation equation, the current stays the same. So there's no frequency scaling regardless of the device's speed. ECL devices maintain relatively constant power dissipation and therefore high device reliability at higher frequencies.

The termination power dissipation for ECLinPS-Plus devices, using 50 Ohms to Vtt, is typically 13 mW per output. The total power dissipation is the sum of the power dissipation of the chip plus the termination. Chip dissipation is fixed and constant over the frequency range per specification. For example, the MC10EP16 has a typical I_{EE} of 24 mA. Therefore, the chip P_D is 79 mW (24 mA x 3.3 V). Now add the termination dissipation of 13 mW, and the total power dissipation (P_D) totals 92 mW, even at 3.4 GHz.

The ECLinPS-Plus Family

The new ECL Plus family features five different types of devices: Buffer Chips, Signal Dividers/Clock Generation Chips, Translators, Line Drivers, and traditional Logic.

"All devices that include 100EP in their part number," notes ON Semiconductor's Veto, "are both voltage and temperature compensated, whereas the 10EP designation denotes voltage compensation only. "

One popular chip, the MC10EP016 can divide a signal by any number between 2 and 256 at a frequency of 2.5 GHz with cascading capability.

The MC100EP139 Signal Divider/Clock Generation Chip divides the clock signal by 2/4 and also by 4/5/6. It generates two differential outputs for each of the two divider chains. The product family includes several other devices currently available with more signal dividers and clock generation chips scheduled to be released in the next year.

The ECLinPS-Plus family features a rich selection of basic logic chips that include devices such as the 4-input OR/NOR (MC10/100EP01), the 2-Input Differential AND/NAND (MC10/100EP05), the Differential 2-Input XOR/XNOR (MC10/100EP08), the Dual Differential 2:1 Multiplexer (MC10/100EP56), or the Dual Differential 4:1 Multiplexer (MC10/100EP57).

"The MC100EPT23 Dual Differential PECL to TTL Translator is the fastest translator available," says Veto. The family includes a wide selection of translators including all industry standard TTL or CMOS outputs. LVDS Translators are planned for availability in 2000.

In addition to the MC10EP16 and MC10EP89 Differential Line Drivers mentioned above, the ECLinPS-Plus line includes several additional line drivers, and more will be introduced next year.

For the most up to date information about available parts and specifications, please visit the ON Semiconductor website at: www.onsemi.com.

Summary

The new ECLinPS-Plus family of high-speed logic products offers rich opportunities for telecommunications equipment manufacturers. The telecommunciations community is already buzzing about the performance characteristics of the new series including higher speed, tighter jitter performance, faster edge rates, reduced system noise, and advanced line driving capabilities. And many of the new ECLinPS-Plus parts have been designed as direct pin replacement upgrades for their earlier ECLinPS-Lite counterparts.

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